

CLAIMS

What is claimed is:

1. A method for transmitting packets among processing nodes within a data processing system, wherein said data processing system includes a plurality of processing nodes connected to each other via an interconnect, said method comprising:

initiating a request transaction from a master node to a plurality of receiving nodes;

generating a write counter number to be associated with said request transaction;

receiving a combined response from said receiving nodes by said master node;

sending a data packet from said master agent to an intended one of said receiving nodes according to said combined response; and

initiating a new request transaction, along with a new write counter number, immediately after said data packet has been sent without waiting for an acknowledgement from said intended receiving node.

4. The method of Claim 1, wherein said data processing system is a symmetric multiprocessor system.

1 5. An apparatus for transmitting packets among processing nodes within a data
2 processing system, wherein said data processing system includes a plurality of processing
3 nodes connected to each other via an interconnect, said apparatus comprising:

4 means for initiating a request transaction from a master node to a plurality
5 of receiving nodes;

6 means for generating a write counter number to be associated with said
7 request transaction;

8 means for receiving a combined response from said receiving nodes by said
9 master node;

10 means for sending a data packet from said master agent to an intended one
11 of said receiving nodes according to said combined response; and

12 means for initiating a new request transaction, along with a new write
13 counter number, immediately after said data packet has been sent without waiting
14 for an acknowledgement from said intended receiving node.

1 6. The apparatus of Claim 5, wherein said generating means further includes a write
2 counter for generating a new write counter number for each request transaction.

1 7. The apparatus of Claim 5, wherein a number of bits within said write counter
2 number = $\log_{10}(\text{number of nodes within said data processing system})/\log_{10}2$.

1 8. The apparatus of Claim 5, wherein said data processing system is a symmetric
2 multiprocessor system.